

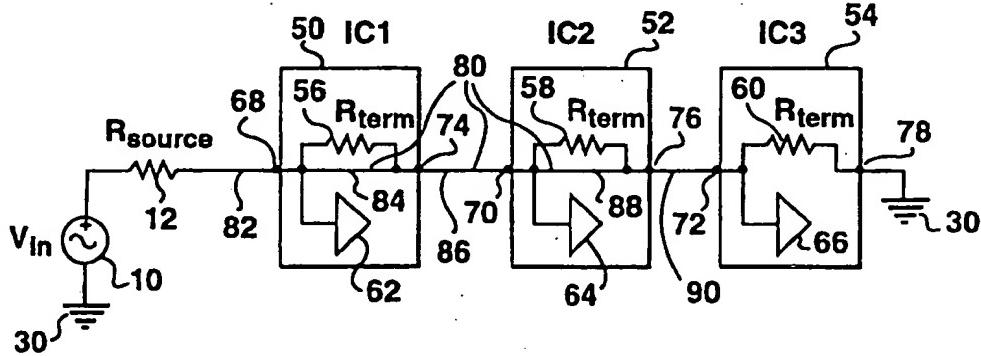


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H03H 7/38, G06F 13/40	A1	(11) International Publication Number: WO 00/28661
		(43) International Publication Date: 18 May 2000 (18.05.00)

(21) International Application Number: PCT/CA99/01033	(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
(22) International Filing Date: 3 November 1999 (03.11.99)	
(30) Priority Data: 09/188,530 10 November 1998 (10.11.98) US	
(71) Applicant (<i>for all designated States except US</i>): GENNUM CORPORATION [CA/CA]; 970 Fraser Drive, Burlington, Ontario L7L 5PS (CA).	
(72) Inventors; and	
(75) Inventors/Applicants (<i>for US only</i>): GUPTA, Atul, Krishna [CA/CA]; Apartment 1102, 950 Warwick Court, Burlington, Ontario L7T 3Z5 (CA). TOFFOLON, Dino [CA/CA]; 11 Earldawn Court, Stoney Creek, Ontario L8G 4N6 (CA).	Published <i>With international search report.</i>
(74) Agent: BERESKIN & PARR; 40 King Street West, 40th floor, Toronto, Ontario M5H 3Y2 (CA).	

(54) Title: BUS THROUGH TERMINATION CIRCUIT



(57) Abstract

A system of resistive end termination and transmission line routing is disclosed for matching the impedance of an IC load to that of a signal source and a transmission line. Each integrated circuit has an internal termination resistor designed to match the characteristic impedance of the transmission line and preferably also the impedance of the source. When the source drives multiple IC devices on a printed circuit board, the devices are cascaded in a chain with the internal resistors of all but the last IC device in the chain bypassed by a short circuit underneath the device, so that a continuous transmission line is provided to the last IC device. The last IC in the chain, which does not have a short circuit underneath it, provides the necessary resistive termination by simply connecting the appropriate pin to a common reference in the circuit. Each integrated circuit has first and second internal termination resistors, the first resistor designed to match the characteristic impedance of the first transmission line and the second resistor designed to match the characteristic impedance of the second transmission line.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Larvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

Title: BUS THROUGH TERMINATION CIRCUITFIELD OF THE INVENTION

The present invention relates to the field of data bus communication, cable drivers, line drivers, buffers, and integrated circuit or monolithic technology. In particular, the present invention relates to a system for eliminating analog or digital signal reflections by way of resistive end terminations in integrated circuits.

BACKGROUND OF THE INVENTION

Impedance matching of an electrical load to the impedance of a signal source and the characteristic impedance of a transmission line is often necessary to reduce reflections by the load back into the transmission line. As the length of a non-terminated transmission line increases, reflections become more and more problematic. When high frequency signals are transmitted or passed through even very short transmission lines, such as printed circuit board (PCB) traces, a resistive termination is typically inserted at the load to avoid reflections and degradations in performance.

When the load comprises one or more integrated circuit devices, the terminal resistor may be either internal or external to the integrated circuit device. The placement of a resistor outside an integrated circuit device results in an additional stub or short transmission line between the resistor and the integrated circuit device. External resistors are also relatively bulky, and so they undesirably increase the required footprint or area for an application. On the other hand, resistors which are internal to an integrated circuit device do not allow for the flexibility of being removed. This is of particular concern when multiple integrated circuit devices are being fed by the same signal along a common transmission line, because the source and transmission line will see a parallel combination of the internal resistors, resulting in an impedance mismatch. Furthermore, when a signal is transmitted or passed to

multiple integrated circuit devices, the transmission line along which the signal passes typically must bend, curve, or turn around each integrated circuit device. These bends, turns, and curves can cause impedance discontinuities in the characteristic impedance of the transmission line,
5 and further result in impedance mismatches.

Thus, there is a need for an integrated circuit resistive end termination and transmission line routing system for applications incorporating integrated circuits on a PCB that provides for accurate impedance matching, minimal reflections, efficient signal routing, and a
10 minimal application footprint.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a system of resistive end termination and transmission line routing for matching the impedance of an IC load to that of a signal source and a transmission line. Each
15 integrated circuit has an internal termination resistor designed to match the characteristic impedance of the transmission line and preferably also the impedance of the source. When the source drives multiple IC devices on a printed circuit board, the devices are cascaded in a chain with the internal resistors of all but the last IC device in the chain bypassed by a
20 short circuit underneath the device, so that a continuous transmission line is provided to the last IC device. The last IC in the chain, which does not have a short circuit underneath it, provides the necessary resistive termination by simply connecting the appropriate pin to a common reference in the circuit. The signal is preferably routed in a straight or
25 direct line as it passes underneath each bypassed IC device and as it passes from one IC device to the next, so as to avoid impedance transitions caused by sharp bends or angles.

Applications requiring differential signal paths can also be accommodated. For differential applications, first and second
30 complementary signal sources feed each IC device along a chain by way of first and second transmission lines respectively. Each integrated circuit has

first and second internal termination resistors, the first resistor designed to match the characteristic impedance of the first transmission line and preferably also the impedance of the first source, and the second resistor designed to match the characteristic impedance of the second transmission
5 line and preferably also the impedance of the second source. The transmission lines bypass the resistors in each IC device except the last IC device in the chain so that continuous transmission lines are provided to the last IC device. The first and second resistors of the last IC device are terminated by shorting them together. Again, the first and second
10 transmission lines preferably pass underneath each bypassed IC device and from one IC device to the next in a straight line.

Thus, in a first aspect the present invention provides a transmission line circuit comprising: (a) a circuit board having at least one layer; (b) a signal source for providing a signal, said signal source having a source impedance; (c) a transmission line running along said circuit board for transmitting the signal, said transmission line having a characteristic line impedance; (d) one or more integrated circuit (IC) devices including one chain-ending IC device, each of said one or more IC devices being positioned along said circuit board so as to receive the signal from said
15 signal source by way of said transmission line, and each of said IC devices having an INPUT pin, an IN/TERM pin, and an internally located resistor coupled between said INPUT pin and said IN/TERM pin, said resistor having a resistive value which matches said line impedance; (e) said transmission line being connected to the INPUT pin and the IN/TERM
20 pin of each of said one or more IC devices except the chain-ending IC device, so that the internal resistor of that device is bypassed by said transmission line; and (f) said transmission line further being connected to the INPUT pin of the chain-ending IC device, and the IN/TERM pin of the chain-ending IC device being connected to a reference.
25

In another aspect, the present invention provides a transmission line circuit comprising: (a) a circuit board having at least one layer; (b) a first signal source for providing a first signal, said first signal

source having a first source impedance; (c) a second signal source for providing a second signal complementary to said first signal, said second signal source having a second source impedance equal to the first source impedance; (d) a first transmission line running along said circuit board
5 for transmitting the first signal, said first transmission line having a first characteristic line impedance; (e) a second transmission line running along said circuit board for transmitting the second signal, said second transmission line having a second characteristic line impedance equal to the first characteristic line impedance; (f) one or more integrated circuit
10 (IC) devices including one chain-ending IC device, each of said one or more IC devices being positioned along said circuit board so as to receive the first signal from said first signal source by way of said first transmission line and to receive the second signal from said second signal source by way of said second transmission line, each of said IC devices having a first
15 INPUT pin, a first IN/TERM pin and a first internally located resistor coupled between said first INPUT pin and said first IN/TERM pin, said first resistor having a resistive value which matches said first line impedance, each of said IC devices further having a second INPUT pin, a second IN/TERM pin and a second internally located resistor coupled
20 between said second INPUT pin and said second IN/TERM pin, said second resistor having a resistive value which matches said second line impedance; (g) said first transmission line being connected to the first INPUT pin and the first IN/TERM pin of each of said one or more IC devices except the chain-ending IC device, so that the first internal resistor
25 of that device is bypassed by said first transmission line; (h) said second transmission line being connected to the second INPUT pin and the second IN/TERM pin of each of said one or more IC devices except the chain-ending IC device, so that the second internal resistor of that device is bypassed by said second transmission line; and (i) said first transmission
30 line further being connected to the first INPUT pin of the chain-ending IC device, said second transmission line further being connected to the second INPUT pin of the chain-ending IC device, and the first IN/TERM

pin and the second IN/TERM pin of the chain-ending IC device being connected to one another.

Further features and advantages of the invention will appear from the following description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, which illustrate preferred embodiments of the present invention:

Figure 1 shows an application in which an integrated circuit device has an external resistive termination according to the prior art.

Figure 2 is a transmission line model of the transmission line stub of Figure 1.

Figure 3 shows an application in which an integrated circuit device has an internal resistive termination according to the prior art.

Figure 4 illustrates an application in which multiple integrated circuit devices each have an internal resistive termination.

Figure 5 shows a modification of Figure 4 in which all but one of the internal resistive terminations are left floating.

Figure 6 shows a first embodiment of the resistive termination and transmission line routing system for an application requiring one or more integrated circuits, in accordance with the present invention.

Figure 7 is an equivalent model of the transmission line circuit of Figure 6.

Figures 8 and 9 illustrate a second embodiment of the resistive termination and transmission line routing system of the present invention for a differential signal path.

DETAILED DESCRIPTION OF THE INVENTION

Transmission lines are designed to transfer signal energy from one location to another. As is well known in the art, a

transmission line, such as a trace or backplane bus on a printed circuit board or a coaxial cable, is often modeled as a number of capacitor-inductor combinations in series with another. The characteristic impedance, Z_0 , of a transmission line is the ratio of the electrical field strength (V/m) to
5 magnetic field strength (A/m) for signals propagating through the transmission line. The characteristic impedance of a transmission line is essentially determined by the materials used for the conductors, the size and spacing of the conductors, and the type of dielectric used between them. At high frequencies, such as in buses for digital systems, the
10 characteristic impedance is predominantly real and is approximately equal to the square root of the per unit length inductance divided by the per unit length capacitance. Thus, the length of the transmission line does not affect the value of its characteristic impedance.

Generally speaking, the time required for a signal to travel
15 from one end of a non-terminated transmission line and back should be considerably less than the transition (i.e. rise and fall) times of the driving signal, as discussed in Sedra, Smith, Microelectronic Circuits (Oxford University Press, 1991). For signals with short transition times (for e.g., 10 nanoseconds or less) and fast propagation speeds (of the order of the speed
20 of light), this will usually not be the case and so a matched or terminated transmission line must be used. Proper termination of an electrical load requires that the output end of the transmission line have an input impedance which is equal to the characteristic impedance of the transmission line as well as the impedance of the source, so that all of the
25 power is provided to the load rather than being reflected by the load back into the transmission line. (Note that it is possible to match the load or output end of a line to the characteristic impedance of the line without also matching the source or input end of the line to the characteristic impedance of the line. However this is usually desirable since it
30 minimizes signal reflections at the source end.) In an integrated circuit device, reflections of transmitted signals may cause degradations in circuit performance (i.e. noise).

To prevent reflections caused by impedance mismatch at the load, termination resistors are used to match the characteristic impedance of the transmission line. The added end termination resistors match the impedance of the transmission line (i.e. the characteristic impedance Z_0) as well as preferably the impedance of the source signal; so that $R_{\text{source}} = Z_0 = R_{\text{term}}$.

As shown in Figure 1, in integrated circuit devices termination resistors are typically placed outside the integrated circuit (IC) or semiconductor chip in the form of a discrete resistor. Referring to Figure 1, a signal source 10 including its effective output resistance 12 is connected to the front-end 14 of a transmission line 16 having characteristic impedance Z_0 . The signal source may be a cable driver, a line driver, or any other signal with a known source resistance. The other end 18 of the transmission line 16 is coupled to a first terminal 22 of termination resistor (R_{term}) 20. Terminal 22 of resistor 20 is coupled to IC device 28 via stub or short trace 26. The other terminal 24 of termination resistor 20 is connected to a common reference 30.

Externally placed resistors allow for flexibility, particularly in devices where several chips are used. However, externally placed resistors considerably increase the required footprint or area for an application. Furthermore, placing the resistor outside the chip results in a stub 26 on the transmission line, and so the signal is not terminated at the very end of the line as it should be.

As shown in Figure 1, the stub 26 is a short section of transmission line which is patched on to the main line and results in a parasitic trace. The transmission line is matched at the point where it meets the terminal 22 of resistor 20. However, due to the stub 26, the signal 10 does not see the same impedance all the way into the chip 28. Figure 2 shows an equivalent circuit model of the transmission line stub 26 in which the short trace includes an inductance L and a capacitance C, as shown. Therefore, the stub 26 results in improper termination and reflections could result.

Placing a terminating resistor 32 inside the IC chip 28, as shown in Figure 3, solves the problems caused by stubs on the transmission line (since stub 26 is eliminated) and, in addition, reduces the required application footprint area. However, this termination technique 5 greatly has been avoided in prior art systems because it reduces the functionality of the IC due to the fact that the termination resistor cannot be removed. The inability to remove the terminating resistor is of particular concern where the source is required to drive multiple integrated circuit devices, since impedance matching in such cases requires 10 that the source see an equivalent impedance equal to its own impedance across all of the IC devices.

Figure 4 illustrates the problem of impedance matching using internal end-termination resistors when multiple integrated circuit chips 28 and 34 are being driven by the same source 10. As shown in Figure 4, 15 IC1 28 has an internal impedance matching resistance 32 of value R_{term} , and similarly IC2 34 has an internal impedance matching resistance 36 of value R_{term} . Because each of IC1 28 and IC2 34 has its own termination resistor, the source sees the parallel combination of all the internal termination resistors (in Figure 4, $R_{term} \parallel R_{term} = \frac{1}{2}R_{term}$), causing a 20 mismatch in impedance. Thus, the IC connections in Figure 4 result in improper or mismatched termination, since the load impedance is half that of the source and reflections consequently result. Similar problems occur when more than two IC devices are being driven by a single source, as is obvious to those skilled in the art. Thus the impedance matching 25 technique of Figure 4 can only be used when the exact number of integrated circuit chips to be driven by a source is known and fixed beforehand — a severe limitation.

A secondary problem which arises when the integrated circuit chips are cascaded as shown in Figure 4 is the cumbersome routing and 30 connections required to route the signal from one IC onto the next. As illustrated by Figure 4, a long trace 38 around IC1 is required to route the signal 10 to IC2 34 which leads to several drawbacks. Long traces increase

the footprint for an application and require additional wiring or trace materials to be used. Second, routing a trace around an IC necessitates bends or turns 39 in the trace which produce discontinuities in the characteristic impedance of the trace. These impedance discontinuities or 5 transitions are difficult to match and will consequently result in further reflections.

One possible solution to the prior art problems associated with internal resistor terminations is to simply connect only the internal resistor 32 of the first IC (IC1 in Figures 4 and 5) to the common reference 10 30 and to leave the other internal resistors floating. This technique, which is illustrated in Figure 5, does provide proper termination, but it still results in poor routing (with the long stub 38 to the next IC remaining).

Figure 6 shows a preferred embodiment of the termination and routing system according to the present invention in which multiple 15 integrated circuit chips IC1 50, IC2 52, and IC3 54 are driven by the same single-ended source 10. Figure 6 shows a signal source 10 with source resistance 12 of value R_{source} which drives three IC chips 50, 52, and 54 each having an internal resistor of value R_{term} (internal resistors 56, 58, and 60 respectively). Although three ICs are shown in Figure 6, the system of the 20 present invention is equally suitable to applications having any number of IC devices. Each of the IC chips IC1 50, IC2 52, and IC3 54 has an INPUT pin (68, 70, and 72 respectively) and a termination or feed through pin, IN/TERM (74, 76, and 78 respectively). The internal termination resistor of each IC device is connected between the INPUT and IN/TERM pins of that 25 device. The high impedance input stages 62, 64, and 66 of the IC products 50, 52, and 54 respectively are also operatively connected to the INPUT terminals 68, 70, and 72 respectively. A "straight" transmission line or trace 80 on a printed circuit board (PCB) preferably passes underneath the IC devices. The trace 80 is preferably straight in that it does not contain 30 bends, turns, or angles as it passes along a layer of the PCB. It will be clear that the term printed circuit board or PCB is intended to embrace any surface or substrate on which integrated circuit devices can be mounted,

including multi-layer circuit boards having a plurality of layers. Note that for ease of reference, the transmission line models 16 of Figures 1, and 3-5 are not shown in Figure 6.

5 The termination and routing system of Figure 6 has four main features.

10 First, each of the IC chips (50, 52, and 54) has an internal termination resistor of value R_{term} which singularly or individually matches the R_{source} impedance 12 of the driving signal and the characteristic impedance Z_0 of the transmission line (not shown). For optimum matching, these internal termination resistors preferably exhibit a tight control in terms of both their absolute value (for example, a tolerance within $\pm 1\%$) and their temperature coefficient (for example within $\pm 200 \text{ ppm}/^\circ\text{C}$).

15 Second, the pinout architecture of each IC device is preferably configured such that the INPUT pin on one side of the IC is lined up directly across from the termination or feed through (IN/TERM) pin on the opposite side.

20 Third, the PCB routing architecture preferably includes a straight transmission line or trace 80 which runs directly underneath each IC, except the last, from its INPUT pin to its feed through/termination pin on the other side so as to bypass the internal termination resistor. As is understood by those skilled in the art, the straight trace 80 may run along one layer or several layers of the PCB, the former being preferable so as to minimize the use of conductive vias in the PCB. Therefore, the IC devices 25 are all positioned on the circuit board so that the INPUT and IN/TERM pins of the devices all line up along the trace 80. In order to avoid or minimize the inclusion of conductive vias in the circuit board (which can potentially give rise to further signal reflections), the trace 80 is preferably on the same layer of the PCB as the IC devices.

30 Fourth, the IN/TERM pin on each IC can be used either as a feed through pin to pass the signal on to the next chip or as a termination connection when the IC is positioned as the last device in a chain. The

IN/TERM pin of the last IC device is connected to a common reference, which in the illustrated embodiment of Figure 6 is the reference 30.

The topology of the present invention significantly reduces reflections and routing from one IC chip to another. When an IC 5 device is not the last in the chain, its internal resistor is bypassed and its IN/TERM pin simply passes the signal on to the next IC. However, when the device is the last in the chain (e.g. IC3 in Figure 6), the IN/TERM pin is connected to a common reference (which in Figure 6 is the reference 30) to provide the proper termination. In addition, because the pins/resistors of the IC devices in the chain are configured in a straight line and allow for a straight PCB trace (transmission line) from the source to each input pin, any stubs with sharp angles and the accompanying impedance discontinuities are eliminated.

An equivalent circuit model of the impedance seen by the 15 source is shown in Figure 7. The resistance R_{term} matches the characteristic impedance Z_0 of the transmission line 80 (i.e. the straight PCB trace) which passes through or underneath all of the IC devices in the chain except the last IC device, IC3. To eliminate reflections at the transmitting end of transmission line 80 the source resistance R_{source} 20 should also match the characteristic impedance Z_0 , as indicated. Sections 82, 84, 86, 88 and 90 of transmission line 80 are similarly labelled in Figures 6 and 7.

The system of the present invention is equally suitable for applications which use or require a fully differential signal path, as shown 25 in the embodiment of Figure 8. In known manner, the differential bus dedicates a pair of transmission lines to two complementary signal sources whose difference forms a differential signal. Referring to Figure 8, a first source 100 having a source resistance 104 drives a cascading IC device chain comprising IC1 110, IC2 112, and IC3 114 via a first transmission line 30 or trace 140. Similarly a second, complementary source 102 having a source resistance 106 equal to source resistance 104 drives the IC devices 110, 112, and 114 via a second transmission line or trace 150. Note that in Figure 8,

as in Figure 6, the transmission line models have been omitted for ease of reference.

For differential source applications, as illustrated in Figure 8, each of the IC chips has two pairs of INPUT and IN/TERM pins. Each of 5 these INPUT-IN/TERM pin pairs is lined up along the transmission lines 140 and 150 respectively in a manner similar to the configuration for single-ended applications. These pins are illustrated for IC1 110 in Figure 8 where a first INPUT pin 128 and a first IN/TERM pin 132 are lined up along transmission line 140, and a second INPUT pin 130 and a second 10 IN/TERM pin 134 are lined up along transmission line 150. The transmission lines 140 and 150 have equal characteristic impedance values. A first internal termination resistance (R_{term}) 116 is connected across pins 128 and 132, while a second internal termination resistance 118 ($\overline{R_{term}}$) is connected across pins 130 and 134. Note that the resistance 116 of value 15 R_{term} , which matches the transmission line 140 and the resistance 118 of $\overline{R_{term}}$ which matches the transmission line 150 are equal.

Referring to Figure 8, all of the IC devices except the last have their INPUT and IN/TERM pins shorted by traces 140 and 150, thus bypassing the internal resistors. The traces 140 and 150 do not continue 20 underneath the last IC device, IC3 114 in Figure 8, which has its IN/TERM pins (136 and 138 for IC3) shorted together to create a node 160 which acts as a virtual ground and at which the two differential signals cancel one another. A decoupling capacitor 170 from the node 160 to a the reference 30 can optionally be used to remove any common mode reflections.

25 Figure 9 shows an exemplary transmission line circuit 200 on a circuit board 280, for an application with a differential driving signal path. The differential circuit of Figure 9 shows the preferred pinout configuration for IC devices 202 and 204 in which the INPUT pins 210, 212, 220, and 222 are directly across from the IN/TERM pins 214, 216, 224, and 30 226 respectively. In addition, IC devices 202 and 204 are positioned or placed such that pins 210 and 214 of device 202 and pin 220 of device 204 are in electrical contact with trace 240, and pins 212 and 216 of device 202

and pin 222 of device 204 are in electrical contact with trace 250. Because device 204 is positioned as the last device in the IC chain, traces 240 and 250 do not continue underneath IC device 204, and so IN/TERM pins 224 and 226 of IC 204 are not directly connected to traces 240 and 250 respectively
5 (i.e. they are connected through an internal resistor).

The traces 240 and 250 transmit the complementary inputs 300 and 302 respectively to the IC devices. The traces 240 and 250 pass underneath IC device 202 and any other IC device which is positioned in "front of" IC device 204, as illustrated at 245 and 255 in Figure 9. The on-chip or internal input termination resistors of the differential configured IC devices are connected in such a manner that, by simply shorting the pins 224 and 226 of the last device 204 on the bus, a proper impedance matched termination is achieved. Also, as shown in Figure 9, the signals from pins 260 of IC devices 202 and 204 are directed to the appropriate 10 application outputs 270. As illustrated, the traces 240 and 250 run along the same layer 290 of circuit board 280) that the IC devices (202 and 204) are positioned or mounted upon.
15

Thus the present invention simply requires that the location of the last or the terminal IC device on the circuit board or backplane be fixed for a given application. Multiple IC devices can then be placed ahead 20 or in front of the last IC device in the direction of the signal source along the preferably straight transmission line trace (or traces for differential signal paths). In addition, any IC device having the bypass-able termination resistor and pinout architecture of the present invention can be placed at any position in the chain without affecting the matching of 25 impedance to the line. If only one IC is required in an application, it is simply connected and positioned as the last device.

In accordance with the present invention, the integrated circuit devices or chips are cascaded in such a way that only one IC in the 30 chain provides the termination, no stubs result, and the routing from chip to chip is clean. The present invention provides an elegant implementation which allows for proper resistive end termination which

matches the impedance of a load to that of a source and a transmission line. Furthermore, the system of the present invention eliminates the need for external end terminations, allows for multiple IC devices to be cascaded efficiently with straight transmission line signal routing, and

5 therefore minimizes reflections caused by stubs and/or impedance mismatch. As a result, the functionality of internal termination resistors and signal routing used in applications having cascading IC devices is greatly improved. Preferably, the internal termination resistors in each device also have a tight control both in absolute value as well as

10 temperature coefficient, to further improve the matching of impedance and elimination of reflections.

While preferred embodiments of the invention have been described, it will be realized that the embodiments disclosed are illustrative and not restrictive, and that all changes within the meaning
15 and scope of the invention are intended to be embraced by the appended claims.

WE CLAIM:

1. A transmission line circuit comprising:
 - (a) a circuit board having at least one layer;
 - (b) a signal source for providing a signal, said signal source having a source impedance;
 - 5 (c) a transmission line running along said circuit board for transmitting the signal, said transmission line having a characteristic line impedance;
 - (d) one or more integrated circuit (IC) devices including one chain-ending IC device, each of said one or more IC devices being positioned along said circuit board so as to receive the signal from said signal source by way of said transmission line, and each of said IC devices having an INPUT pin, an IN/TERM pin, and an internally located resistor coupled between said INPUT pin and said IN/TERM pin, said resistor having a resistive value which matches said line impedance;
 - 10 (e) said transmission line being connected to the INPUT pin and the IN/TERM pin of each of said one or more IC devices except the chain-ending IC device, so that the internal resistor of that device is bypassed by said transmission line; and
 - (f) said transmission line further being connected to the INPUT pin of the chain-ending IC device, and the IN/TERM pin of the chain-ending IC device being connected to a reference.
- 25
2. A transmission line circuit according to claim 1 wherein the INPUT pin and the IN/TERM pin of each of said IC devices are located directly across from one another on each IC device.

3. A transmission line circuit according to claim 2 wherein the source impedance matches the line impedance.
4. A transmission line circuit according to claim 3 in which there are at least two IC devices.
5. A transmission line circuit according to claim 4 wherein said IC devices are positioned on said circuit board in a manner such that said transmission line runs along said circuit board in a straight line.
6. A transmission line circuit according to claim 4 wherein said IC devices are positioned on a single layer of said circuit board and said transmission line runs along the same layer of said circuit board.
7. A transmission line circuit according to claim 4 wherein the INPUT pin of each of said one or more IC devices is coupled to a high impedance input stage of that device.
8. A transmission line circuit according to claim 4 wherein said circuit board is a printed circuit board and said transmission line is a printed circuit board trace.
9. A transmission line circuit according to claim 4 wherein said reference is the most negative supply voltage in said transmission line circuit.
10. A transmission line circuit according to claim 4 wherein said signal has transition times of 10 nanoseconds or less.
11. A transmission line circuit according to claim 4 wherein the internally located resistors of said IC devices have an absolute value tolerance of $\pm 1\%$ and a temperature coefficient within $\pm 200 \text{ ppm}/^\circ\text{C}$.

12. A transmission line circuit comprising:
- (a) a circuit board having at least one layer;
 - (b) a first signal source for providing a first signal, said first signal source having a first source impedance;
 - 5 (c) a second signal source for providing a second signal complementary to said first signal, said second signal source having a second source impedance equal to the first source impedance;
 - (d) a first transmission line running along said circuit board for transmitting the first signal, said first transmission line having a first characteristic line impedance;
 - 10 (e) a second transmission line running along said circuit board for transmitting the second signal, said second transmission line having a second characteristic line impedance equal to the first characteristic line impedance;
 - 15 (f) one or more integrated circuit (IC) devices including one chain-ending IC device, each of said one or more IC devices being positioned along said circuit board so as to receive the first signal from said first signal source by way of said first transmission line and to receive the second signal from said second signal source by way of said second transmission line, each of said IC devices having a first INPUT pin, a first IN/TERM pin and a first internally located resistor coupled between said first INPUT pin and said first IN/TERM pin, said first resistor having a resistive value which matches said first line impedance, each of said IC devices further having a second INPUT pin, a second IN/TERM pin and a second internally located resistor coupled between said second INPUT pin and said second

- 18 -

IN/TERM pin, said second resistor having a resistive value which matches said second line impedance;

5 (g) said first transmission line being connected to the first INPUT pin and the first IN/TERM pin of each of said one or more IC devices except the chain-ending IC device, so that the first internal resistor of that device is bypassed by said first transmission line;

10 (h) said second transmission line being connected to the second INPUT pin and the second IN/TERM pin of each of said one or more IC devices except the chain-ending IC device, so that the second internal resistor of that device is bypassed by said second transmission line; and

15 (i) said first transmission line further being connected to the first INPUT pin of the chain-ending IC device, said second transmission line further being connected to the second INPUT pin of the chain-ending IC device, and the first IN/TERM pin and the second IN/TERM pin of the chain-ending IC device being connected to 20 one another.

13. A transmission line circuit according to claim 12 wherein the first INPUT pin and the first IN/TERM pin of each of said IC devices are located directly across from one another on each IC device, and the second INPUT pin and the second IN/TERM pin of each of said IC devices are 25 located directly across from one another on each IC device.

14. A transmission line circuit according to claim 13 wherein the first source impedance matches the first line impedance and the second source impedance matches the second line impedance.

15. A transmission line circuit according to claim 14 in which

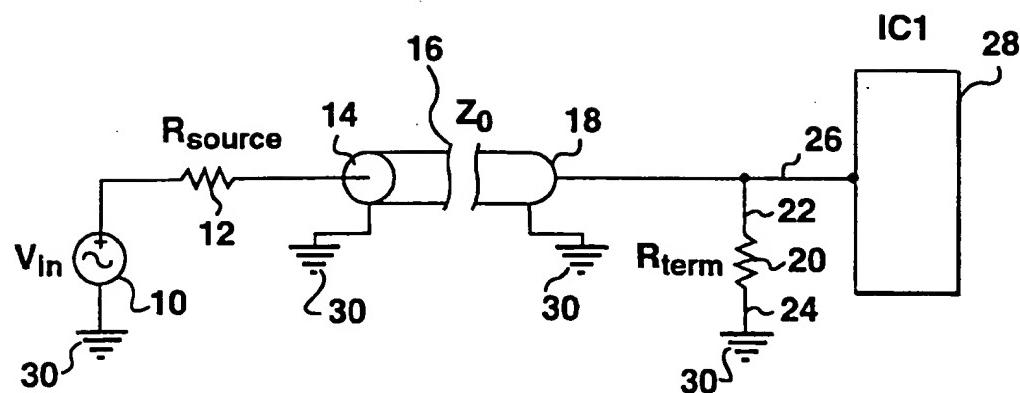
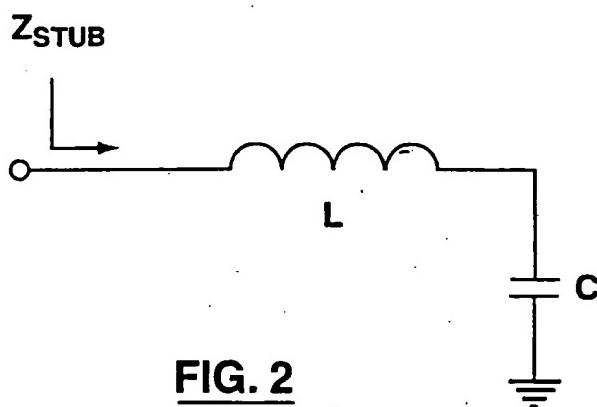
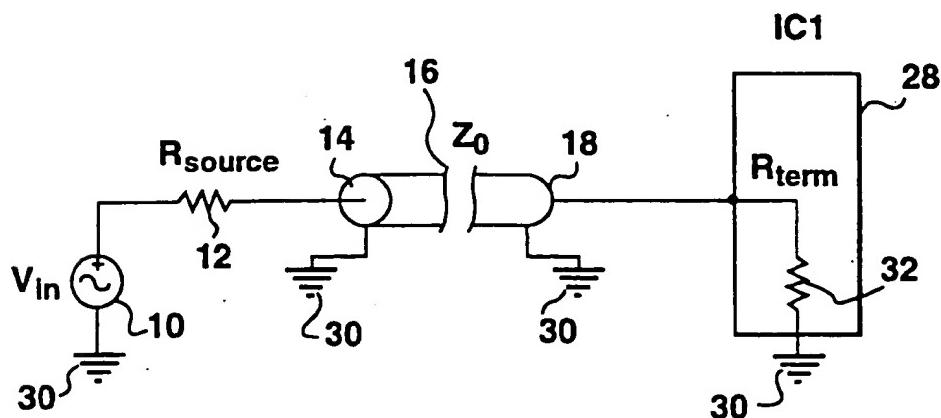
there are at least two IC devices.

16. A transmission line circuit according to claim 15 wherein said IC devices are positioned on said circuit board in a manner such that said first and second transmission lines run along said circuit board in a straight line.
17. A transmission line circuit according to claim 15 wherein said IC devices are positioned on a single layer of said circuit board and said first and second transmission lines run along the same layer of said circuit board.
- 10 18. A transmission line circuit according to claim 15 wherein the first and second INPUT pins of each of said one or more IC devices is coupled to a high impedance input stage of that device.
19. A transmission line circuit according to claim 15 wherein said circuit board is a printed circuit board and said first and second transmission lines are a printed circuit board traces.
20. A transmission line circuit according to claim 15 wherein said first and second signals have transition times of 10 nanoseconds or less.
21. A transmission line circuit according to claim 15 wherein a first terminal of a capacitor is connected to the node formed by the connection of the first IN/TERM pin and the second IN/TERM pin of the chain-ending IC device and the second terminal of said capacitor is connected to a reference.
22. A transmission line circuit according to claim 15 wherein the first and second internally located resistors of said IC devices have an absolute value tolerance of $\pm 1\%$ and a temperature coefficient within \pm

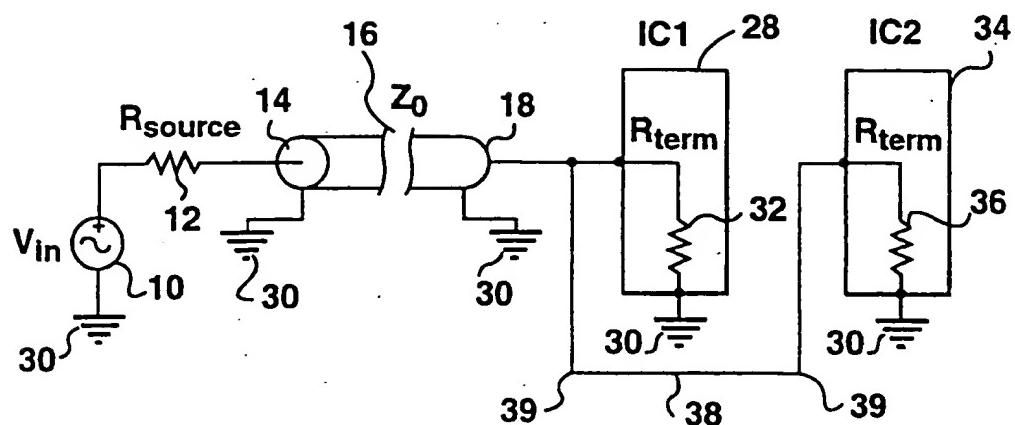
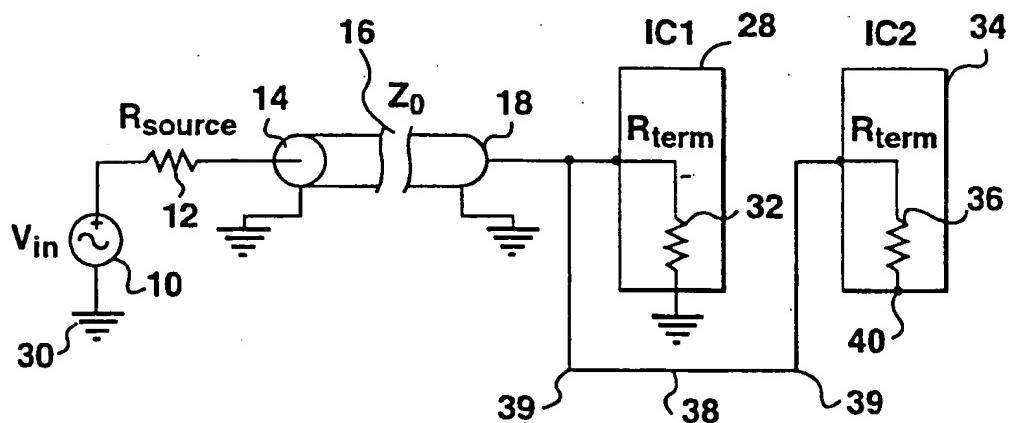
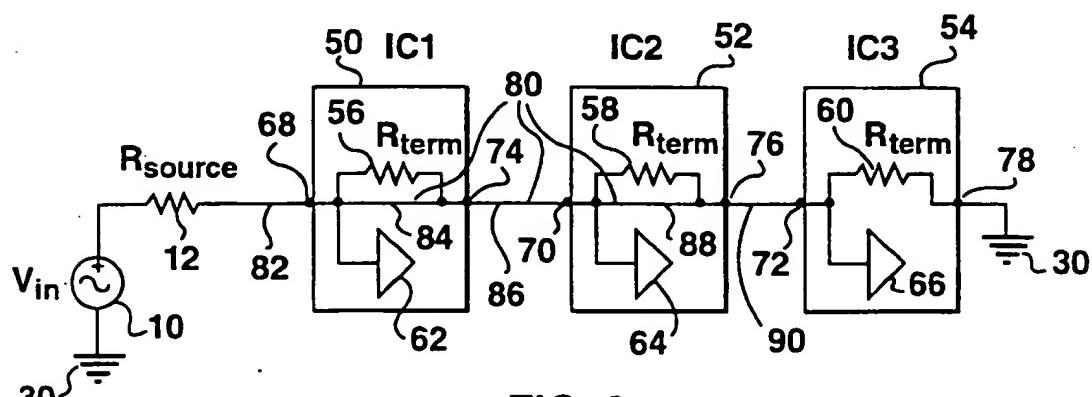
- 20 -

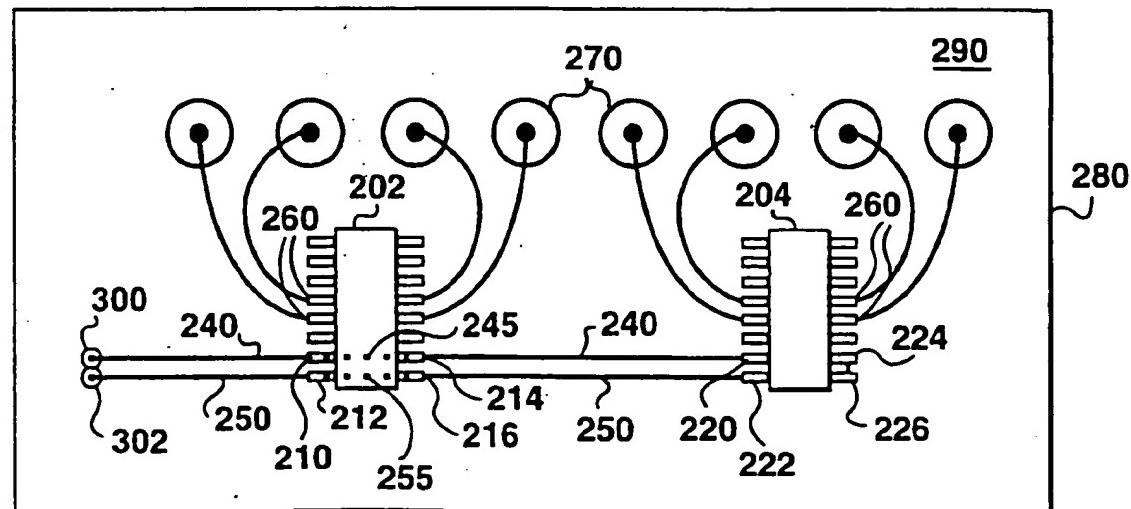
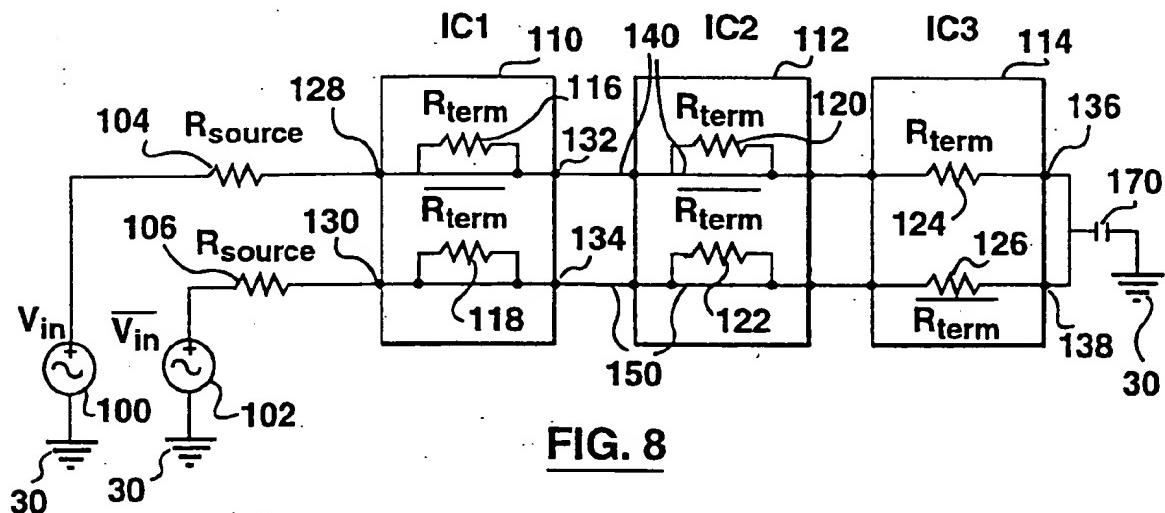
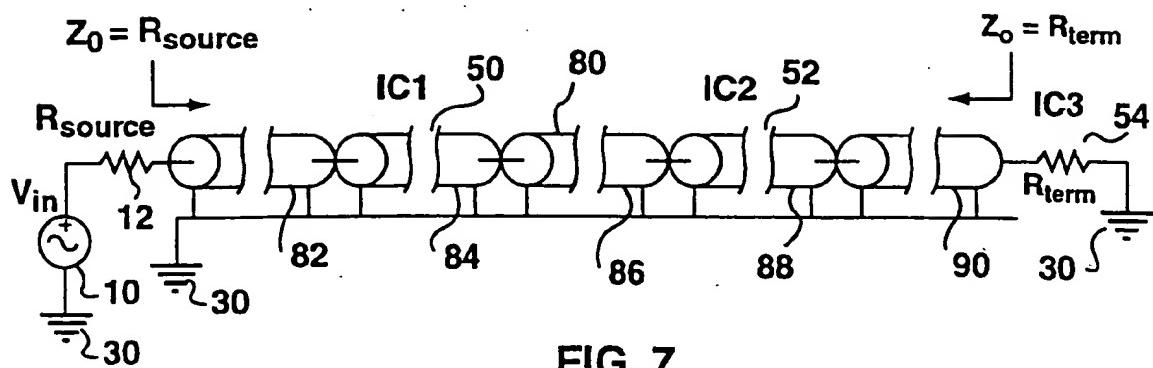
200 ppm/°C.

1 / 3

**FIG. 1 (Prior art)****FIG. 2****FIG. 3 (Prior art)**

2 / 3

**FIG. 4****FIG. 5****FIG. 6**



INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 99/01033

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03H7/38 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03H G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 721 497 A (NOVAK VIT F) 24 February 1998 (1998-02-24) column 1, line 35 -column 2, line 56 column 4, line 20 -column 5, line 65; figures 1,2 -----	1-5,8, 12-16



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

31 January 2000

04/02/2000

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 000 nl,
Fax: (+31-70) 340-3016

Authorized officer

Coppieters, C

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int'l. Application No

PCT/CA 99/01033

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5721497 A	24-02-1998	NONE	